ABSTRACT OF THE DISCLOSURE

[0031] A CMOS semiconductor product employs a first doped well of a first polarity and a second doped well of a second polarity opposite the first polarity, each formed laterally separated within a semiconductor substrate. The first doped well is further embedded within a third doped well of the second polarity that further separates the first doped well from the second doped well. The third doped well provides latch-up resistance for a pair of MOS transistors formed within the first doped well and the second doped well.